Optimized Virtex-4 FPGA Self Hosting Configuration Management

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Driving Causes

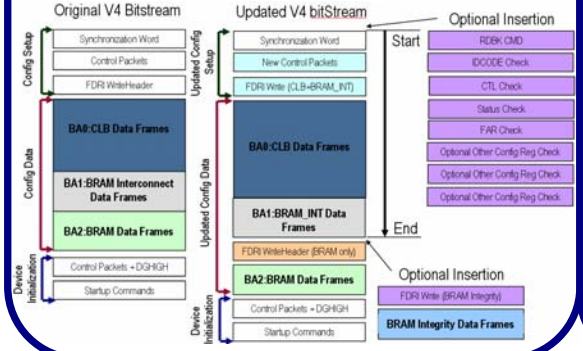
- Cost!
- Flexibility
- Risk Mitigation

Future Development

- Official software support
- Column or row based operation
- Multiple device chained setup
- One click IP insertion with TMRTool

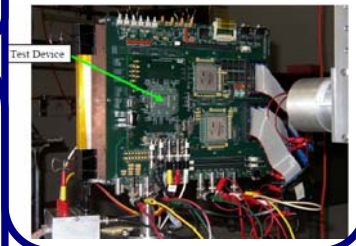
Soft Setup

- Bitstream manipulation
  - Store all readback commands
  - Store all SEFI check commands
  - SEU detection and correction is simply counter
  - BRAM data integrity error detection and correction
- Independent module that can be plugged into any design
- Constraints separating TMR domains to eliminate DCE or MBU



Test Environment

- Texas A&M Cyclotron Institute & Lawrence Berkeley Nation Lab
- Source: Ne, Ar



IP Core Performance

Device	Detection and Correction Cycle Time*	Resource Utilization (% of available device slices)**
SX55	**0.28 Sec**	**3.5%**
FX60	**0.26 sec**	**3.4%**
FX140	**0.6 sec**	**1.3%**
LX200	**0.6 sec**	**1.0%**

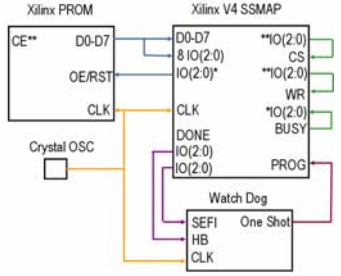
*Design running with SMAP 8 Bit interface at 20MHz. Divide the cycle time by four if SMAP32 interface is implemented.
**TMR IP with full device readback. Divide the number by 2 for scrub only TMR version IP.

Test Results

LET (MeV * cm^2/mg)	Flux (particles/cm^2 sec)	Expected SEFI Cross Section (cm^2)	Self Scrubber SEFI Cross Section (cm^2)	Self Scrubber Failure Cross Section (cm^2)
5.3	5.5×10^{3}	2.82×10^{-7}	4.17×10^{-7}	NA
5.3	5.27×10^{3}	2.82×10^{-7}	2.00×10^{-7}	NA
7.27	3.3×10^{4}	4.93×10^{-7}	6.17×10^{-7}	1.44×10^{-6}
7.27	1.2×10^{4}	4.93×10^{-7}	6.86×10^{-7}	6.86×10^{-7}
7.27	3.88×10^{3}	4.93×10^{-7}	4.93×10^{-7}	2.46×10^{-7}
9	4.8×10^{4}	6.38×10^{-7}	8.50×10^{-7}	7.00×10^{-7}
9	8.6×10^{3}	6.38×10^{-7}	7.83×10^{-7}	3.23×10^{-7}

Test Design Setup

- DUT: XQV4LX200
- Supporting devices (Not irradiated):
  - Configuration storage: XCF32P + XCF32P
  - Watchdog: XC2VP70
- Design:
  - VHDL based
  - Triplication by Xilinx TMRTool
  - Source code available upon request
  - Functionality test: DCM
- Functional Monitor:
  - Monitor DCM outputs to ensure device function
  - Monitor number of PROG reset



*Denotes weak pull up on signal
**Denotes weak pull down on signal

IP Core Implementation

- SMAP8 interface
- Support for generic memory with data valid input
- All FF periodically reset
- No configuration commands stored in IP
- Support SRL16/LUTRAM implementation
- SMAP, POR, GSIG, FAR SEFI detection
  - GSIG and POR SEFI detected though watchdog circuit
- Heartbeat signal to indicate Core status.
- Optional Error detection with CRC16 or CRC32
  - Correction occurs after mismatching CRC